Abstracts

RF LDMOS characterization and its compact modeling

Jaejune Jang, O. Tornblad, T. Arnborg, Qiang Chen, K. Banerjee, Zhiping Yu and R.W. Dutton. "RF LDMOS characterization and its compact modeling." 2001 MTT-S International Microwave Symposium Digest 01.2 (2001 Vol. II [MWSYM]): 967-970 vol.2.

This paper presents characterization of power LDMOS using device simulation and analytical modeling. Features of the LDMOS such as graded channel and quasi-saturation effect which result in a peculiar behavior on capacitance and nonlinear LDD resistance are analyzed and modeled using device simulation. A compact model for LDMOS is implemented in HSPICE based on additional lumped elements, combined with the BSIM3 MOSFET model.

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